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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,132	07/22/2003	Joseph M. Jeddeloh	501304.01	8276

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EXAMINER	
SORRELL, ERON J	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,132	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,5,6,8,9,13,14,17,18,21,22,24,26,28,29,32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige et al. (U.S. Patent No. 6,477,614 hereinafter "Leddige" in view of Cheung (U.S. Pub No. 2004/0216018).

3. Referring to apparatus claims 1 and 8, and system claims 13 and 24, Leddige teaches a computer system, comprising:

a central processing unit ("CPU") (see item 101 in figure 1);

a system controller coupled to the CPU (see item 111 in figure 1), the system controller having an input port and an output port (see bi-directional interface connecting item 111 to bus 120);

an input device coupled to the CPU through the system controller (see item 123 in figure 1);

an output device coupled to the CPU through the system controller (see item 122 in figure 1);

a storage device coupled to the CPU through the system controller (see item 131 in figure 1)

a memory bus on which memory requests are provided (see item 300 in figure 3);

a plurality of memory devices (see items labeled "MEMORY DEVICE" in figure 3); and

a memory hub (see item 320 in figure 3) , comprising:

a link interface for receiving memory requests for access to at least one of the memory devices (see item 310 in figure 3);

a memory device interface coupled to the memory devices (see item 321 and 322 in figure 3), the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (see paragraph bridging columns 3 and 4);

a switch for selectively coupling the link interface and the memory device interface (see lines 11-52 of column 8);

and a communications link coupled between the system controller and at least one of the plurality of memory modules

for coupling memory requests and data between the system controller and the memory modules (see bus connecting item 111 to item 113 in figure 1).

Leddige fails to teach the hub further comprises a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations.

Cheung teaches in an analogous system a DMA controller located on a memory module (see paragraph 11 on page 2), the DMA engine generating memory requests for access to at least one memory device to perform DMA operations (see paragraph 10 on page 1).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the memory module of Leddige with the above teachings of Cheung. One of ordinary skill would have been motivated to make such modification in order to provide testing and verification of components as suggested by Cheung (see paragraph 10 on page 1) in addition to relieving the memory hub of burdensome data transfers freeing it to work on other tasks.

4. Referring to apparatus claims 2 and 9, and system claims 14 and 26, the combination of Leddige and Cheung teaches the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device (see figure 7 of Leddige and paragraph 11 on page 2 of Cheung).

5. Referring to apparatus claim 5 and system claims 21 and 32, Leddige teaches the plurality of memory devices is a bank of memory devices simultaneously accessed during a memory operation (see MEMORY DEVICES in figure 3 and paragraph bridging columns 3 and 4).

6. Referring to claim 6, and system claims 22 and 33, Leddige teaches the plurality of memory devices comprise synchronous dynamic random access memory devices (see lines 17-31 of column 2).

7. Referring to system claim 17 and 28, Leddige teaches a plurality of memory modules (see items 210a, 211a, and 212a in figure 3) are included in the memory system and a first memory module (see item 210a) of the plurality of memory modules is coupled to the memory bus (note that memory bus 300 is only

connected to module 310a) and the remaining memory modules of the plurality are coupled in series with the first memory module (see interfaces 311-314 in figure 3).

8. Referring to system claim 18 and 29, Leddige teaches a plurality of memory modules are included in the memory system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface (see figure 5).

9. Claims 7,12,23, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige in view of Cheung as applied to claims 1,8,13, and 24 above, and further in view of Schmidt (U.S. Patent No. 6,782,465).

10. Referring to claims apparatus claim 7 and 12, and system claims 23 and 34, the combination of Leddige and Cheung teaches the DMA engine comprises (see Cheung figure 2):

an address register for storing a starting memory address for a DMA operation (see paragraph 16 on page 2);

a target address location for storing a target address of a location to which data is to be moved in the DMA operation (see paragraph 16 on page 2);

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation (see paragraph 16 on page 2).

The combination of Leddige and Cheung fails to teach the DMA controller further comprises a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

Schmidt teaches a DMA controller comprising the above next register (see lines 5-18 of column 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Leddige and Schmidt with the above teachings of Schmidt in order to increase the rate of memory transfers as suggested by Schmidt (se liens 7-10 of column 2).

11. Claims 4,11,20, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige and Cheung as applied to claims 1,8,13, and 24 above, and further in view of "Throughput Expansion with FET Based Crossbar Switching" (hereinafter Jones).

12. Referring to apparatus claims 4 and 11, and system claims 20 and 31, the combination of Leddige and Cheung fails to teach the switch is a crossbar switch.

Jones teaches a crossbar switch with "very low propagation delays…that can fit in any environment requiring greater bandwidth (see paragraph bridging pages 2 and 3)."

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Leddige and Cheung with the above teachings from Jones to increase throughput through the hub as suggested by Jones.

13. Claims 15,16,25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige in view of Cheung as applied to claims 1,8,13, and 24 above, and further in view of Frame et al. (US Pub. No. 2004/0243769 hereinafter "Frame").

14. Referring to claims 15,16,25, and 27, the combination of Leddige and Cheung fails to teach a communications link comprises a high-speed optical memory bus and wherein the link interface of the memory hub comprises an optical memory bus

interface circuit for translating optical signals and electrical signals.

Frame teaches, in an analogous system, the above limitation (see paragraph 15 on page 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Leddige and Cheung with the above teachings of Frame in order to further increase bandwidth through the system.

Response to Arguments

15. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
January 7, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER

1/8/06